What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal; and

a monitor terminal connected to said test mode circuit and outputting said test mode signal.

2. The nonvolatile semiconductor memory device according to claim 1, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

3. The nonvolatile semiconductor memory device according to claim 1, further comprising a column switch connected to

said column decoder and said bit line.

4. The nonvolatile semiconductor memory device according to claim 1, wherein said monitor terminal is a monitor pad.

5. The nonvolatile semiconductor memory device according to claim 1, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

6. A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal; and

a monitor terminal connected to said word line and outputting the test mode signal given to said word line.

7. The nonvolatile semiconductor memory device according

to claim 6, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

8. The nonvolatile semiconductor memory device according to claim 6, further comprising a column switch connected to said column decoder and said bit line.

9. The nonvolatile semiconductor memory device according to claim 6, wherein said monitor terminal is a monitor pad.

10. The nonvolatile semiconductor memory device according to claim 6, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

11. A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

a test cell having plural memory cells which are connected to said word lines and are also connected to a test word line;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and

applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal;

a test decoder connected to said test mode circuit and applying the voltage for a test to said test word line in response to said test mode signal; and

a monitor terminal connected to said test word line and outputting the voltage for a test applied to said test word line.

12. The nonvolatile semiconductor memory device according to claim 11, further comprising a select line connected to the drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

13. The nonvolatile semiconductor memory device according to claim 11, further comprising a column switch connected to said column decoder and said bit line.

14. The nonvolatile semiconductor memory device according to claim 11, wherein said monitor terminal is a monitor pad.

15. The nonvolatile semiconductor memory device according to claim 11, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

16. A nonvolatile semiconductor memory device comprising:

a memory cell array having plural memory cells and arranged in an array shape by connecting these memory cells to plural bit lines and word lines;

a test cell having plural memory cells which are connected to said word lines and are also connected to a test word line;

plural address input terminals inputting addresses thereto;

a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among these address input terminals;

a row decoder connected to said test mode circuit and applying a voltage for a test to all said word lines in response to said test mode signal;

a column decoder connected to said test mode circuit and setting all said bit lines to a non-selecting state in response to said test mode signal;

a test decoder connected to said test mode circuit and applying the voltage for a test to said test word line in response to said test mode signal; and

a test mode detecting circuit connected to said test word line and detecting the voltage for a test applied to said test word line and outputting the detecting result.

17. The nonvolatile semiconductor memory device according to claim 16, further comprising a select line connected to the

drain of a memory cell, and a regulator connected to this select line and said test mode circuit and giving a predetermined bias electric potential to the drain of said memory cell.

18. The nonvolatile semiconductor memory device according to claim 16, further comprising a column switch connected to said column decoder and said bit line.

19. The nonvolatile semiconductor memory device according to claim 16, further comprising a control signal input terminal for receiving a control signal, and a control circuit connected to this control signal input terminal.

20. The nonvolatile semiconductor memory device according to claim 16, wherein the nonvolatile semiconductor memory device further comprises a data input-output terminal, and the detecting result of said test mode detecting circuit is outputted from said data input-output terminal.